A DEDICATED CONTROLLER FOR ADAPTIVE OPTICS L3CCD DEVELOPMENTS

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Abstract: We present the dedicated controller being developped in the framework of the OPTICON JRA2 programme "Fast Visible Detectors for adaptive optics" [1]. The CCD developped within this programme is a highly specialized chip using E2V's Low light level charge coupled device (L3CCD) technology capable of outstanding capabilities [2]. It is not possible to extrapolate existing controller techniques since the chip needs radiofrequency signals (more than 10MHz) for clocking, and gives a high frequency video output. The compactness is of prime importance in order to deal with these high frequency signals and is also important for future integration in next generation adaptive optics systems. Developping such a controller is very challenging and needs to use innovative techniques to fullfill the requirements.We will quickly summarize the JRA2 and detector requirements, derive the controller requirements, present guidelines concept of the controller, point out the challenges of this controler.

Key words: Wavefront sensor, charge coupled device (CCD) controller, Low light level charge coupled device (L3CCD)

1. OPTICON AND THE JRA2 DETECTOR (CCD220)

The Optical Infrared Co-ordination Network for Astronomy (OPTICON) is a European Union funded thematic network bringing together national funding agencies and users with common interests in optical and infrared adstronomy. The aim of the OPTICON Joint Research Activity 2 (JRA2) is to develop Visible detectors fully matching the requirements of Adaptive Optics (AO) wavefront sensors for 10m class telescopes that do not yet exist: current detectors have frame rates which are too slow and which are too

noisy for the second generation of AO systems [1]. The developped CCD (named CCD220) main characteristics are summarized in table 1.

Table 1. CCD220 main characteristics

item	specification
Detector format	240x240 pixels of 24 µm – 8 L3 outputs – Frame transfert
Frame rate	25-1500 Hz
Parallel transfer rate	10 Mlines/s
Read noise	<1e$^-$ at 1.2 kHz

2. IMPACT OF REQUIREMENTS ON CCD CONTROLLER

2.1 Data throughput

Assuming a 1 500 Hz frame rate with necessary overheads to shift the charges from storage section to serial register, the necessary pixel rate with 8 outputs is 13.7 Mpixels/s per output, giving a throughput of ~110Mpixels/s. The data is digitized with 14bits, giving a usefull transfert rate of 220Mbytes/s. This is much higher than a standard transmission and a classical computer bus can accept. Several solutions were considered for data transmission, including networked standards (Gigabit ethernet, IEEE1394, USB2.0, etc…). The Cameralink industrial standard has been selected. It has been developped by major camera suppliers for large and/or fast sensors and a lot of grabbers and other accessories are avalaible on the market. The cameralink full specification exhibits a data troughput of 680Mbytes/s with standard grabbers on PCI-X bus or PCI-Express.

2.2 Sequencer resolution

Using Frequencies up to 13.7 MHz for the phases generation gives a phase period of 73 ns. This has a big impact on the necessary sequencer resolution. Since the chip is using a L3 output, it is necessary to adjust the phases of the CCD very precisely in order to have a good electron multiplication in the gain register [3]. A this frequency, the phase scale is 5°/ns. A 20° phase shift in a case of a sine HV phase gives 6% of phase voltage decrease. This effect can be canceled by increasing the HV clock voltage, but it is limited by the HV phase breakdown voltage. Also, since the

Comment: At

multiplication occurs when the sine is not at its maximum level, small jitters in the serial clock will produce gain variations. Therefore a sequencer resolution down to 1ns would be necessary. The foreseen technical solution is to use several very fast master clocks (up to 400MHz) finely skewed from each other with a specialized circuitry.

2.3 Data acquisition

At a rate of 13.7 Mpixels/s, it is very tricky to build a correlated double sampling (CDS) system that has a suitable performance. The goal is to have 14 bits dynamics since analog to digital converters sufficiently fast are avalaible now only with this dynamics. The baseline is to use an integrated analog front end (AFE) with ebedded CDS, built by classical integrated circuit suppliers. This has the advantage of offering a very compact system (insentitive to EMI/RFI) with a lot of built-in features such as programmable gain amplifiers. The other alternative is to use an oversampled system and a digital CDS. Using selected wheighted coefficients, it would also be possible to reduce the overall readout noise [4][5]. These two approaches will be developped in parallel.

Comment: embedded

2.4 Phases drive

The required bandwidth for any periodic square like signal is given by the classical formula :

$$BW = \frac{0.35}{\tau}$$

Comment: This is the formula of the equivalent frequency at those rise and fall time , the bandwidth of the device should be higher (one octave at least) to be sure that it works at a good point.

where τ is the rise/fall time. Serial phases require 5ns rise time this gives a required bandwidth of 70MHz and with a 15V amplitude a slew rate of 3kV/µs.

The parallel phases drive have less constraints of bandwidth but since the phases of a CCD behave electrically as capacitors, it's necessary to drive a large capacitor at high speed. The parallel phase capacitance will be approximatively 2nF, giving an impedance of 8Ω at 10MHz. This is probably the main issue of the controller since it is necessary then to be able to provide several amperes of current to the CCD. To avoid current flow through the VSS pin, a symetrical 2 phases parallel register will be used to balance the current flows.

Comment: (almost pure reactive)

The HV phase needs a 50V amplitude sine drive. The sine wave is prefered to avoid thermal dissipation in the chip. This is very hard to achieve

Comment: Peut-etre evoquer le fait que du point de vue thermique ce n'est pas non plus aise car a cause des courants forts et des dI/dt tres faibles la self parasite est influente , ce qui nous oblige a regrouper les CI et donc concentre les sources de dissipation de chaleur.

with classical circuits because of the necessary current drive of the HV phase. The impedance of the HV phase at 13.7 MHz is 116 Ω, therefore the peak current in the phase is 430 mA. The driver dissipation in this case is several watts. The solution is to use a resonnant clocking system that uses the energy transfert between an inductor and the capacitor of the phase. Using this technique the driver power dissipation drops to less than 1W.

3. THE CONTROLLER DESIGN

3.1 General architecture

Comment: architecture

Dealing with such high frequencies is very uncommon for an astronomical CCD controller. The classical approach consisting of putting all the drive electronics into a box far away (one meter) from the cryostat head is not applicable in this case. With such high bandwiths, a strict impedance matching would be necessary to avoid ringings of the signals trough the cables. But a CCD phase is a pure reactive load, therefore impedance matching is not possible. The only way to proceed is to arrange all the drive electronics close to the detector.

3.2 Inductance of PCB traces

The inductance of a pcb trace is given by the formula :

$$LT \approx 0.2L\left[\ln\left(\frac{L}{w+h}\right)+1.2+0.22\left(\frac{w+h}{L}\right)\right]$$

where LT is the inductance in nH, L the length of the track, w the width and h the thickness of copper all in millimeters. This shows a weak dependance of trace thickness (10nH/cm for a 200µm track, 7nH/cm for a 1mm track). This series inductance will create overshoots and undershoots since it makes an oscilator with the phases capacitance. These overshoots are proportionnal to the current variation, and in the case of parallel phases, a small wire of a few cm adds an unacceptable overshoot. Figure 1 shows a SPICE simulation of the effect of a 4nH parasitic inductance due to a 0.5 cm wire or PCB trace on the drive waveform of the parallel phases of CCD220.

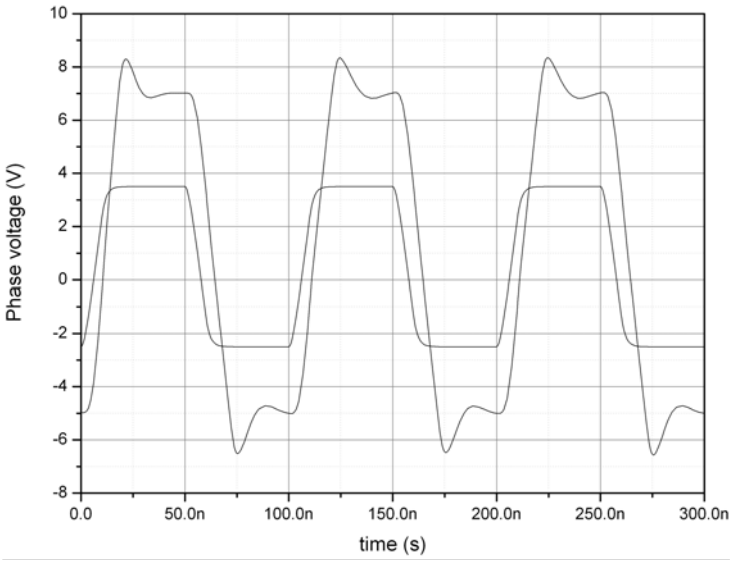

Figure 1. Effect of a 4nH parasitic inductance on the parallel clocks. Lowest amplitude signal is the drive waveform, highest is the clock signal (the buffer has a gain of 2)

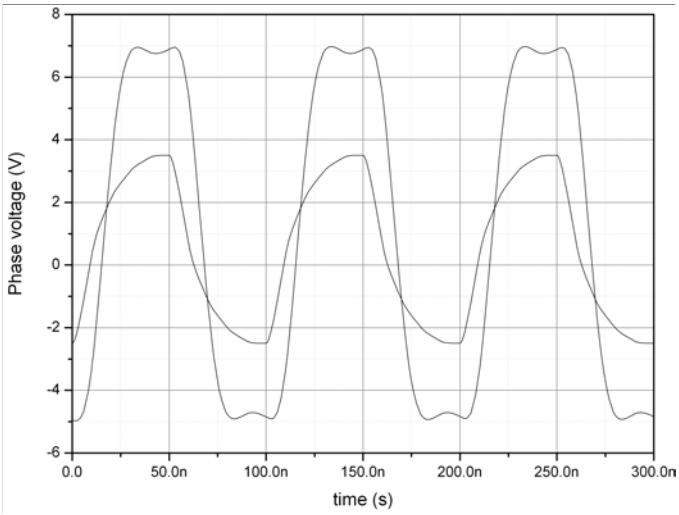

Figure 2. overshoot cancelation (large trace) with a controlled drive shape (small trace) and a parasitic capacitance of 10nH.

The only way to reduce the parasitic inductance is to increase the mutual inductance of the phase drive track and its returning path by minimizing the

distance of these two tracks. Practically, the inductance can be divided by a factor 2.5 to 5. Another method, which could be used in conjunction with the previous one, is to use a shape controlled drive waveform to counterbalance the oscillation, but in this case the phase drivers can't be simple switches and have to be amplifiers. Figure 2 shows the effect of controlled drive with a parasitic inductance of 10nH. Finally, driving CCD220 parallel phases with sine waves is also possible due to the symetric 2 phases structure and would have the advantage of minimizing clock induced charge [6].

4. CONCLUSION

Designing a CCD controller for CCD220 needs the use of high frequency techniques usually not necessary in CCD controllers due to the low readout speed. A particular care has to be taken with wire length that introduce parasitic inductance, especially when high current flows are present. Classical CCD controllers approaches, with separate control electronics connected to the CCD head by long wires are widely used in astronomy but are not applicable in this case. A fully integrated approach must be used to place all the CCD drive electronics close to the chip and therefore in close conjuction with mechanical and cryogenic design.

5. REFERENCES

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