The Opticon JRA2

Fast Detectors for AO

Opticon Executive Meeting
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Name

Signature

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Management work package (WP1) activity report

1. UPDATED LIST OF MEETINGS

Since the first annual report, some additional meetings were held:
- Detector Kick-off meeting: 3-4 March 2005, Chelmsford at the e2v factory.
- Opticon JRA2 discussions with e2v during the Scientific Detector Workshop 2005, Sicily, 19-25 June 2005.

The following meetings are foreseen:
- Detector Design Review, 22-23 September 2005, Chelmsford at the e2v factory.
- next JRA2 general meeting: November 2005 at ESO Garching.

2. LIST OF MILESTRONES/DELIVERABLES

Hereafter is listed the list of milestones and deliverables extracted from the first annual report. The status of each item is showed in the table.

Work package	Milestones/ Deliverables	Project Month	Description	Status
2	M3	18	Concept design review to agree the specification.	Achieved March 05
2	M4	18	Detailed design review of the detector.	Scheduled Sept 05
3	M3A	30	Delivery of detector controller.	On time
3	M3B	30	Complete controller test.	On time
3	D1	30	Controller acceptance report.	On time
4	M1	18	Complete cryogenic system design	Scheduled Sept 05
4	M2	30	Cryogenic system acceptance.	On time

Note that the WP3 activity may suffer from the late delivery of funding from Opticon. If this situation does not change, this could have an impact on the overall schedule of the JRA2.

Detector specification and fabrication work package (WP2) activity report

1- APPLICABLE DOCUMENTS

AD1 Technical specifications for the Adaptive Optics Wavefront Sensor Detector VLT-SPE-ESO-14690-3320, issue 3, 19 April 2005
AD2 Statement of work for the Adaptive Optics Wavefront Sensor Detector, VLT-SOW-ESO-14690-3383, issue 4, 15 April 2005.
AD3 Technical and management proposal E2V-PR-679, issue 4, 10 March 2005.

2- DETECTOR REQUIREMENTS

The OPTICON JRA2 science working group set the top level requirements after carefully considering the needs of AO systems for future instruments and their science programs. The following detailed requirements were established:

1. big pixels, square 24μm (goal), to ease the optic design, but not too large to produce excessive dark current (DC) or CTE problems.
2. versatility of a 100% fill factor and 240x240 square grid array of pixels that can be used by any WFS systems: SH, curvature, or pyramid, with or without gaps (guard bands) between subapertures.
3. format size of 240 pixels being a number that is divisible by the number of output nodes, 8, and binning factors and aperture sizes of 1, 2, 3, 4, 5, 6 and meets the minimum pixel requirement of 40 subapertures x 6 pixels/subapertures.
4. low read noise of < 1 e-/pixel and goal of 0.1 e-/pixel.
5. range of operating frame rates from 25frames/s for use when photon starved with faint-NGS (Natural Guide Star) to highest sampling rate of 1.2 kframes/s for use with bright-NGS and LGS (Laser Guide Star).
6. easy to use; eight output nodes each operating at maximum pixel rate of 15 Mpixel/s, that provide a good compromise between the number of connections between the detector and the outside world and operational practicalities such as power dissipation, pixel rates and clocking rates.
7. low image smearing (<5%) when transferring image to store area; an undesirable affect that can be corrected.
8. cosmetically defects free as every defect will either complicate the centroiding or make it impossible to centroid a sub-aperture.
9. good spatial characteristics, PSF < 0.9 pixel FWHM over 460 to 950 nm, to accurately determine where the photons interact.
10. very low Dark current, DC, of < 0.01 e-/pixel/frame at 1200 frames/s and < 0.04 e-/pixel/frame at 25 frames/s to minimize the large errors introduced by the quantum nature of DC; electron is the smallest unit. A single electron of DC creates a large error when centroiding on a small number or single photon. DC includes contributions from clock induced charge (fixed amount per frame readout), image area during exposure (α exposure time), frame store and serial register during readout (α frame read out time).
11. Peltier cooled package for small compact size, maintenance free, and minimal support equipment so that final assembled camera system can fit in the small space volumes usually reserved for AO systems.

12. detection signal limit of 5 ke-. In normal operation, the system will be photon starved as there are not too many bright NGS and the power of laser of LGS will be reduced to a minimum. Well depth and output amplifier dynamic range can be traded to improve other parameters such as higher gain of output amplifier and lower clock amplitudes to transfer charge.
13. linearity of < 2%. Analysis shows that this level of linearity introduces insignificant errors. Linearity can be corrected by a look-up table.

3- DESIGN

The design (Figure 1) is a 24 µm square 240x240 pixels split frame transfer 8-output back illuminated L3CCD, designated as CCD220.
The image and store area are built with metal-buttressed parallel clock structures to enable line shifts of 10 Mlines/s for total transfer time from image to store of 12 µs and low smearing of under 1.5% at 1.2 kframe/s. Two phase clocking was chosen for simplicity, lower power dissipation, and symmetry of drive.

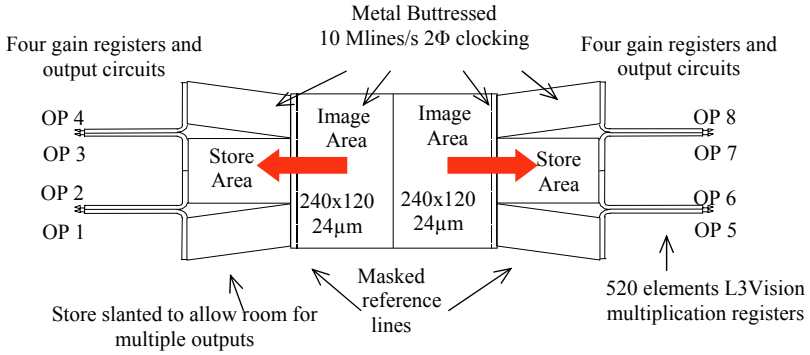


Figure 1. Schematic of CCD220.

The store area is slanted out to make room for the standard serial registers (three phase clocking) to curve around (Figure 2) and provide space for the output circuitry. Each output will have a 520 element 16 µm standard L3Vision gain registers whose gain is controlled by the voltage of the multiplication phase. The output amplifier will be a single stage (Table 1 for specifications) and of similar design that have been employed on recent L3V CCDs. The gain register and output amplifier will be optimized for a gain of 1000, a value typically expected for AO applications, to provide an overall effective read noise of under 0.1e-. The serial registers, gain registers, and output amplifiers are designed to operate up to 15 Mpixel/s to achieve a full frame rate of over 1.5kframes/s.
The baseline device will be built in standard silicon and is low risk with guaranteed delivery of devices that meet minimum requirements. This meets the risk profile of both JRA2, who must produce a design report to the EC on a 2-3 year timescale, and ESO, who require working detectors for their next generation of instruments. A split wafer run will enable two speculative variants to be built. The first is to build devices in deep depletion silicon which will offer much better red response. High red response is important for applications that rely on natural GS such as VLT Planet Finder. The second is to build devices with an electronic shutter to extend the use of the detector to applications such as Rayleigh Laser Guide Star, RLGS, which require shutter times of µs which are difficult to achieve mechanically. RLGS systems offer substantial cost savings and development effort in that they can use commercial available pulsed lasers as opposed to specialized sodium lasers.

Table 1. Specifications of output amplifier.

Feature	**CCD220**
Overall responsivity	1.7 µV/electron
Node capacitance	57 fF
Noise (rms with CDS ~ 15 MHz)	45 electrons
Reset rms noise (dominates without CDS)	100 electrons
Saturation (3V swing at node)	1.0M electrons
Output impedance	350 Ohms
Maximum frequency (settling to 1%) [1]	15 MHz
Maximum frequency (settling to 5%)	25 MHz

No dump gate was included in the design as it was doubtful whether its response time to dump charge would be any faster than simply clocking the serial register, and if included would add excessive capacitance to neighboring registers and add pins to the package resulting in a larger package size and more heat load. Additionally, for deep depletion devices a much wider dump gate would be required to avoid parasitic effects resulting in an even slower dump time.

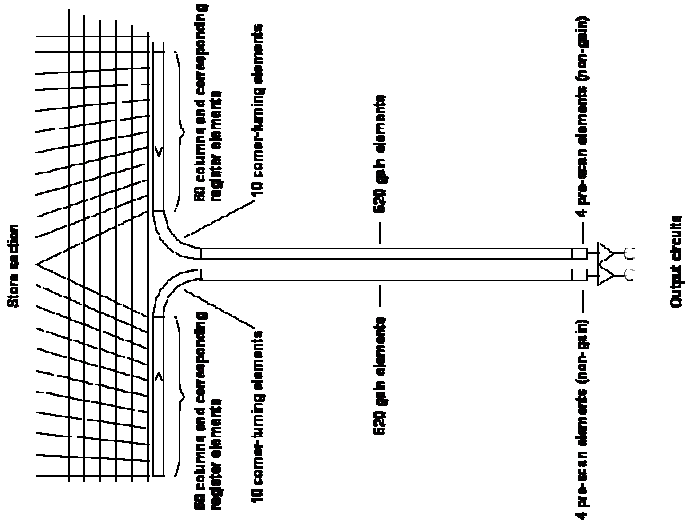


Figure 2. Details of serial and gain register.

As well to reduce pin count, summing wells were not included as it was thought to be acceptable that with low read noise of 0.1e- binning could just as easily be performed off chip.

4- SCHEDULE

The major milestones (Table 2) are CDR in Q3 2005, package review at end 2005, and final device delivery in Q2 2007. Test equipment and camera electronics is being developed by LAM INSU/CNRS and LAOG INSU/CNRS. It will be loaned to e2v for testing. The same test equipment will be used by the IAC (José Javier Díaz) to do acceptance test. ESO are

[1] Load capacitance (external and package) < 10 pF

developing the New General Controller, NGC, to support the CCD220 for deployment on the VLT.

Table 2. Major milestones of CCD220 development.

Milestone	Date
Kick-off meeting	March 2005
CCD220 and Test Equipment Critical Design Review (CDR)	Q3 2005
Package Design Review	End 2005
Mechanical samples delivery	Mid 2006
ESO supplied test equipment delivery	Q3 2006
Devices delivery	Q2 2007

5- CONCLUSION

Several European institutions under the umbrella of OPTICON have formed a very good working relationship with e2v to develop a new 240x240 pixel wavefront sensor detector, CCD220, with subelectron read noise at 1.2kframes/s that will enable future AO systems to provide the image quality and stability to guarantee the success of next generation of instruments on 8 to 10-m class telescope. Baseline development is low risk by extending existing e2v L3Vision technology to multiple outputs and metal buttressing parallel clock structures. In addition higher risk (more speculative) but higher performance devices in deep depletion silicon and with electronic shutter will be developed in parallel. For compactness and low maintenance the CCD is mounted in an optimized Peltier cooled package.
In August 2004, a Call for Tenders was issued for the Development and Supply of 240x240 pixels, very low noise (1e- or less), fast readout (1.2 kframes/s) CCD detectors that meet set requirements. This culminated in a contract between e2v and ESO (responsible of the WP2) in March 2005 to start the detector development. ESO is the contact point for the contact with e2v, the activity is jointly funded by OPTICON and ESO.

Controller work package (WP3) June 2005 activity report

1. RESEARCH & DEVELOPMENT ACTIVITIES

1.1. Introduction

The current period is fully dedicated to the development and fabrication of the final CCD controller. An important update is that the controller will be provided also to E2V for their testing purposes before delivering the chips to the consortium. This will save 270k€ on the initial contract. The development time has been shorten to 15 months after contract signature with E2V for the first controller. A second controller will be delivered to the consortium tests within 3 extra months. The controller design has been reviewed and discussed by the consortium at ESO. The architecture is divided in 7 modules : Analog front end, drivers, sequencer, microcontroller, interface and acquisition system. The 3 first are key developments of the programme.

1.2. Key technological developments

1.2.1. Scope

The CCD chip being developed within the OPTICON JRA2 consortium has several uncommon characteristics. The preliminary design of the chip (named CCD220) has been provided to the consortium at the detector Kick-Off held at E2V's premises in Chelmsford on 3&4 march 2005. The first is the number of L3vision amplifiers, 8 in this case. This will be the first time that a multiple output L3vision chip is produced. The second is the readout speed that implies high frequency drives and high frequency design. We extrapolate the knowledge we gathered for the CCD65 and CCD97 chips for CCD220.

1.2.2. Clocks drivers

CCD 220 needs 13.7 MHz serial phases and 10MHz parallel to be operated at the foreseen frame rate. During the last 3 months we developed technical solutions for the phases drives. Several possible solutions were studied in parallel, from PSPICE simulations to the realization of several prototypes. Now, the prototypes are being under tests and characterization for performance evaluation.

1.2.3. A/D conversion

There is a hard constraint on the performance of the analog to digital conversion of the 8 outputs of the CCD220. Two different technical solutions are presently studied. One is a fast track solution with asics and despite it has a lower performance, it will be the first solution used, to meet the timing constraints with a delivery date to the manufacturer 15 months after the detector kick-off. The second one with higher performance will be realized later on and will be evaluated by the consortium tests (WP5)

1.2.4. Sequencer

The sequencer study did not start yet.

1.3. Classical developments

1.3.1. Microcontroller

The microcontroller and microcode has been fully developed. The first version is fully operational and does not need any further modifications.

1.3.2. Interface

The interface has been developed and is now under tests. The interface is capable of simulating the output of a CCD in order to test the link with the acquisition. Therefore it will be possible to fully characterize it on an early stage of the development.

1.3.3. Acquisition system

The acquisition system has been selected. It is now under performance tests in conjunction with the interface test.

2. REALIZATIONS & TESTS

2.1. microcontroller module

The microcontroller board is the first realized part of the controller. It has been released in April 2005, in advance on the schedule. It has been fully tested and characterized for normal operation and meet all the constraints of the programme.

2.2. Interface module

The interface module has been released in June 2005 in advance on the schedule. It has not been characterized yet and will be on the next weeks.

2.3. Acquisition system

The acquisition system has been released in June 2005 in advance on the schedule. It is now fully operational and is under tests and characterization.

3. ACTIVITY FOR THE NEXT MONTHS

3.1. Research & development activity

Actual research & developments around drivers and analog front end will continue to select the best solutions for the final controller. The driver study is now on the final stage and will be finalized in the next few weeks. The analog front end study is at an early stage and will continue for the next months. We expect to start the sequencer development also in the next months.

3.2. Realization and tests activity

The next weeks will be devoted to characterization and tests of the interface module in conjunction with the acquisition system. The aim is to fully characterize the transmission system and to verify that it is compliant to the needs of the programme. At the same time, the acquisition software development will start. We cannot start new module developments before the chip manufacturer design review since this has a big impact on the remaining controller modules. The design review is foreseen for September 2005.

4. CONCLUSION

For the moment, no big technical issues were encountered. The workpackage 3 is in advance on the schedule. We expect then to be on time for the delivery of the controller to the manufacturer and to the JRA2 consortium.

Cryogenic system work package (WP4) activity report

1. APPLICABLE DOCUMENTS

AD4 CCD 220 Thermal Resistance Modelling Report, date : 6/7/2005, S. Hurrel, e2v internal report.

2. PACKAGE

The devices will be mounted in a compact Peltier cooled package similar to that shown in figure 1. Peltier cooler and package will be custom-designed and able to cool down the CCD sufficiently to meet the dark current requirements over the full operating frame rates. The estimated power dissipation of the CCD at 1.2 kframes/sec (worst case) is shown in Table 1. The Peltier cooler, ceramic chip carrier and CCD will be glued by a thermally conductive epoxy adhesive. The package will be sealed and filled with 0.9 bar of Krypton gas to minimize heat transfer to the outside.

Table1. Estimated total and on-chip power dissipation of CCD220 at 1.2 kframes/s.

Section	Load	Delta V	Mean f	W_{total}	$W_{on\text{-}chip}$
Image	4.2 nF	10 V	185 kHz	78 mW	23 mW
Store	3.6 nF	10 V	370 kHz	133 mW	40 mW
Register	1.5 nF	10 V	13.2 MHz	2.0 W	800 mW
HV	0.4 nF	45 V	13.6 MHz	11.0 W	220 mW
Amplifiers				8x50 mW	400 mW
Total					~1.5 W

The CCD220 die will have four fiducial crosses situated two either side of the device image area, in the region of the bond pads. These will be clearly visible through the package window for alignment purposes such as attachment of lenslet arrays. An AD590 temperature sensor will be glued to the ceramic chip carrier to provide sensor for temperature regulation. The sapphire entrance window will be of a high optical quality (double path wavefront error of < 50nm rms), good surface quality (defects meet 5/2x0,05 DIN3140), and AR coated with transmission > 98% over range 400-950nm.

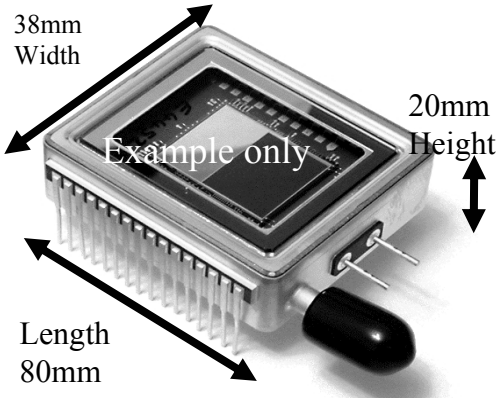


Figure1. Photograph of CCD65 Peltier cooling package. The AO CCD220 detector will use a similar Peltier package. Dimensions shown are the requirements on the maximum package size.

3. THERMAL ANALYSIS

3.1. introduction

3.1.1. Purpose and scope

The purpose of this analysis is to build a thermal model of all the cold head of the CCD220 ESO-WFS package. This model starts by a modelling of the thermal resistance between the water cooling circuit and the back side of the Peltier package. These simulations were also done by e2v using another modelling tool: IcePack. Alternative concepts to the original one are also presented in this document.
The simulations presented here were carried out using the I-deas/TMG software module provided by the UGS software editor, now distributed as a module of " I-deas ® NX Series" called "NX MasterFEM TMG Thermal". We used version 9 of I-deas under Windows XP Operating System. TMG is the thermal module integrated inside the I-deas software distribution.

3.1.2. Applicable documents

CCD 220 Thermal Resistance Modelling Report, date : 6/7/2005, S. Hurrel, e2v internal report.

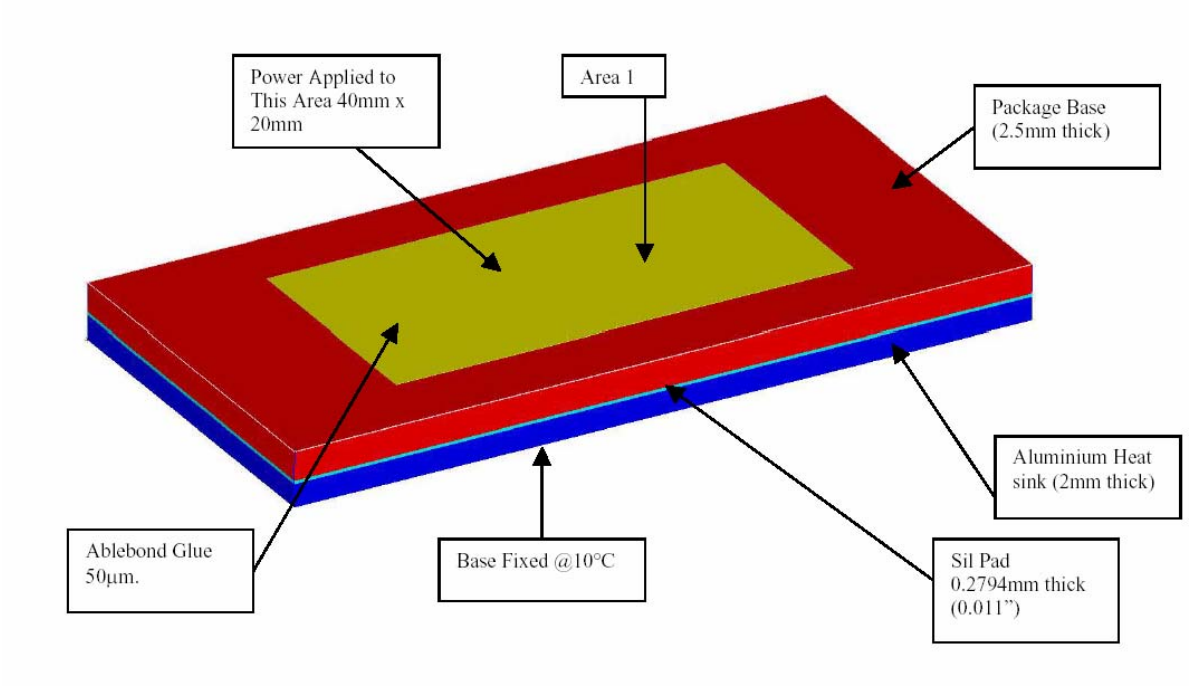
3.2. Assumptions

- Exchanges by thermal conduction only. Effects of radiation and convection neglected.
- Use of the Silpad A2000 0.011" thick between the package and the cooling exchanger in what we called the "original concept". Integration of the cooling circuit inside the package for the alternative concepts.
- Material properties and thickness: same as in "CCD 220 Thermal Resistance Modelling Report", 6/7/2005.
- In this entire document, the water temperature is equal to 10 °C. The VLT water temperature is often under this value, typically 7 °C.

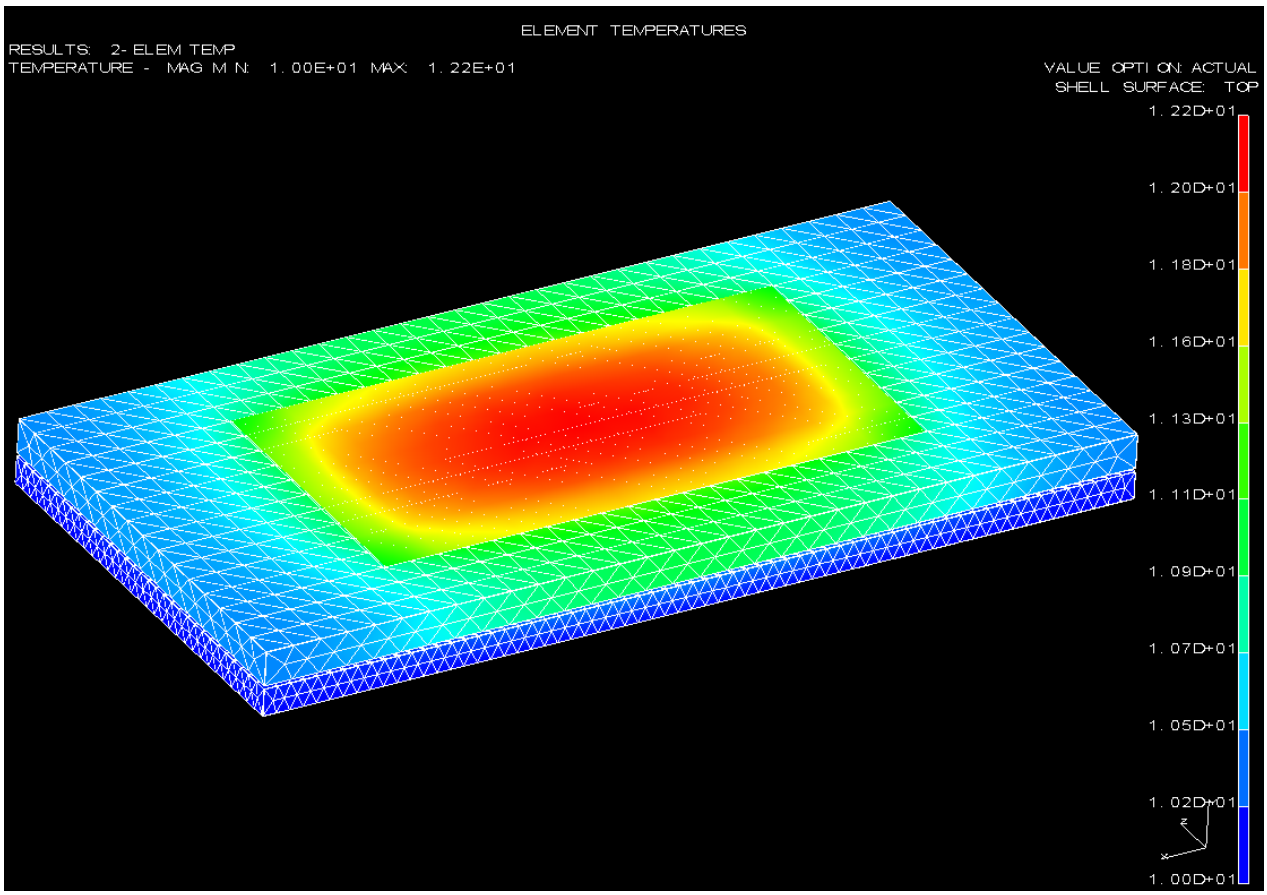
3.3. Original package concept

3.3.1. Geometry

The geometry used for the calculation is identical to what was considered in the e2v thermal report:



3.3.2. 15W applied power



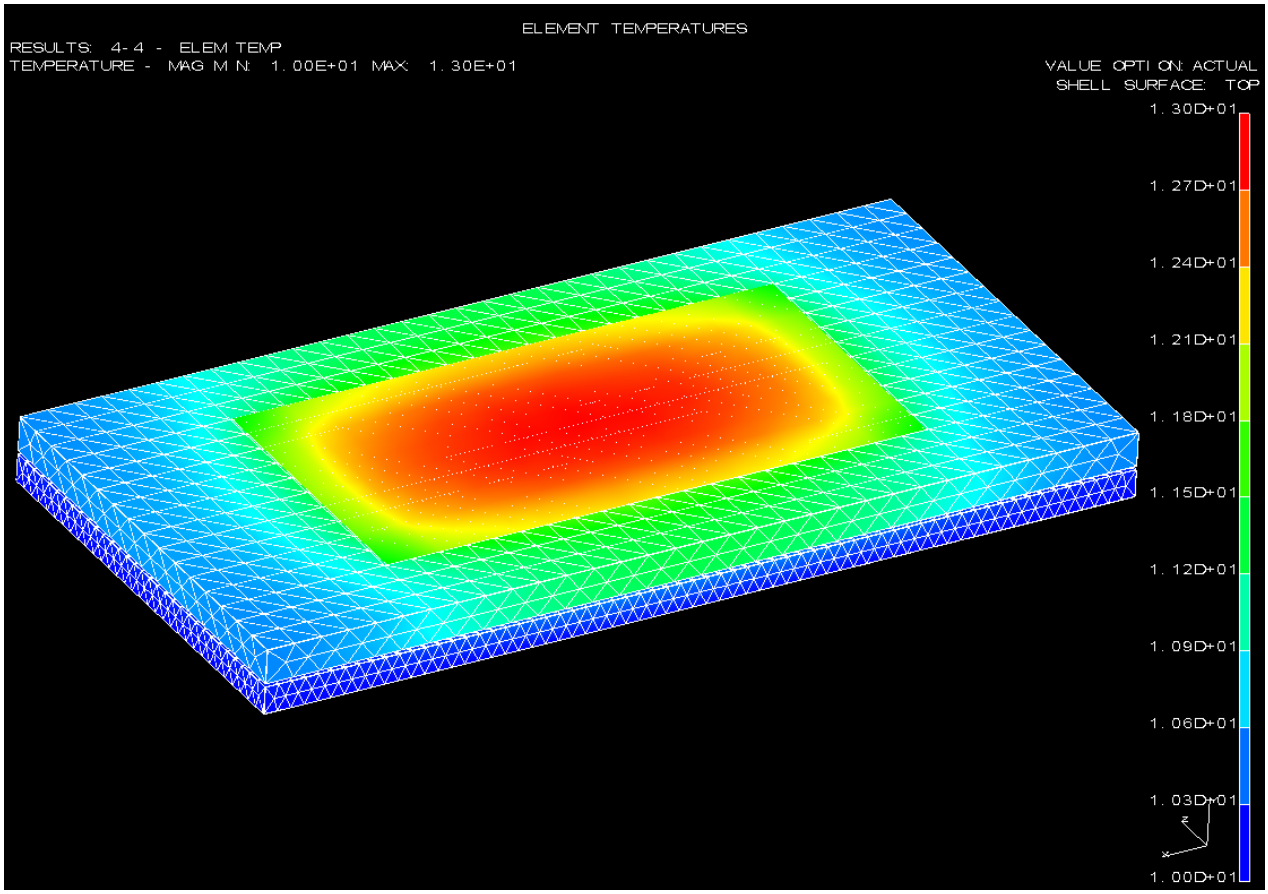
The temperatures at the glue/Peltier interface are:

Min	Max	Average
11.07	12.24	11.87

This allows estimating an equivalent thermal resistance:

$$R_{th} = \frac{T_{av}(°C) - 10}{15} = 0.125\,°C/W$$

3.3.3. 20W applied power



Temperatures at the glue/Peltier interface:

Min	Max	Average
11.43	12.99	12.50

Equivalent thermal resistance:

$$R_{th} = \frac{T_{av}(°C) - 10}{20} = 0.125\,°C/W$$ (same result than with 15W).

3.3.4. Conclusion for the original concept

This study confirms the value of thermal resistance calculated by e2V: **0.125 W/°C**.
Nonetheless, we confirm here that a figure of **0.2 W/°C** can be considered for the thermal resistance between the back side of the package and the interface glue/Peltier.

3.4. Evolution/improvement of this model

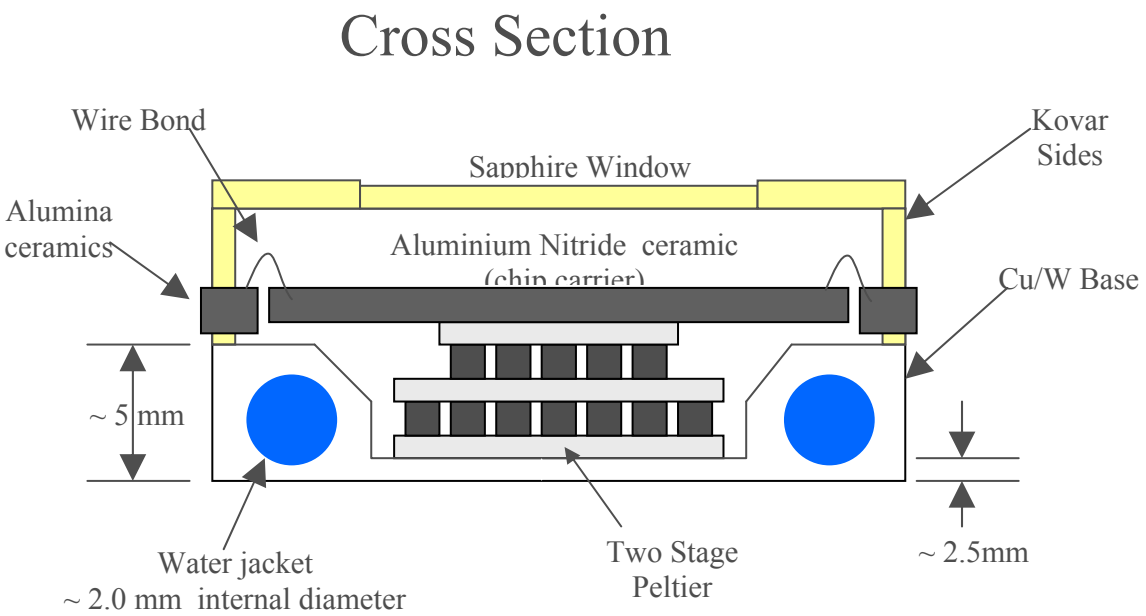
We plan to further improve this thermal model by including the following items:

- Peltier stack and Peltier boundaries conditions
- free convection with the ambient air
- if necessary, radiation between the cold side of the Peltier and the package.
- modelling of the water cooling exchanger (exchanger performances as a function of the water flow).
- cooling of the electronics boards.

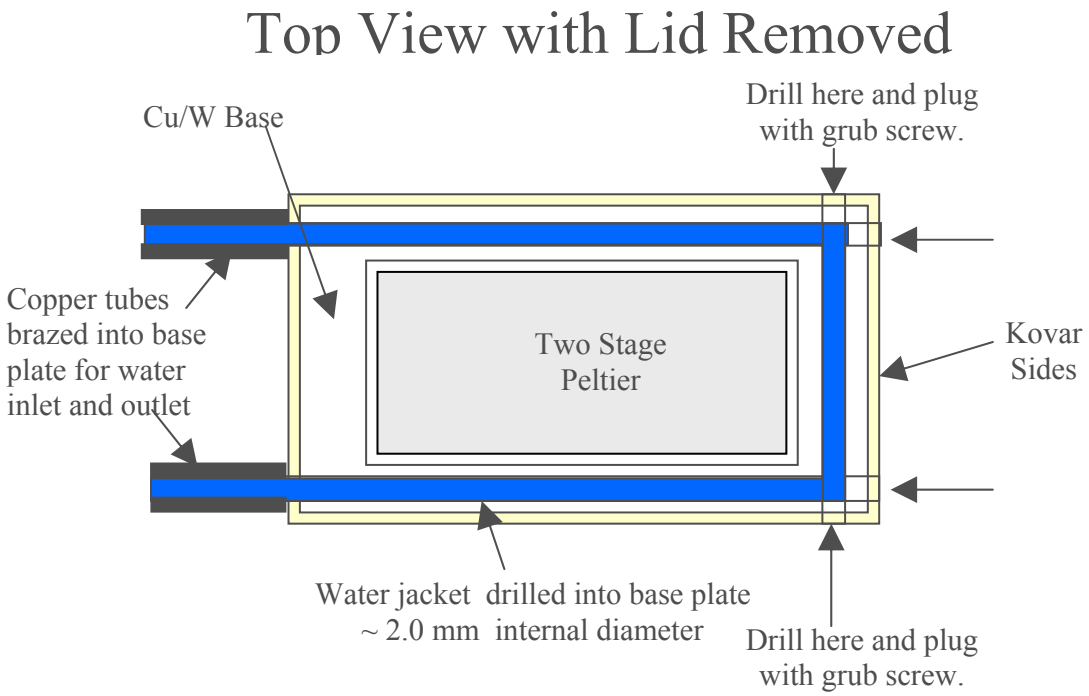
3.5. Alternative design 1: cooling exchanger inside the package

3.5.1. purpose of this design

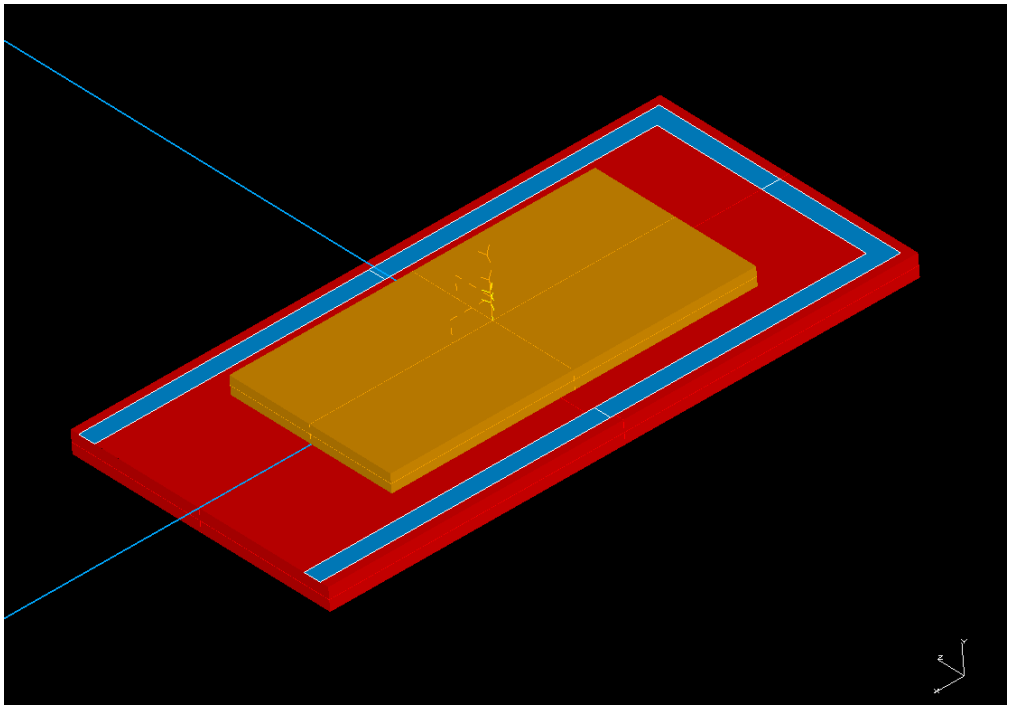
- Why not integrate the heat exchanger into the base plate of the package?
- Advantages:
  - No thermal interfaces allowing a best thermal design.
  - Improves wiring as base plate and water jacket take up less space and final assembly is more compact.
  - Makes assembly easier.



- Water jacket in base plate takes advantage of the unused space below the alumina ceramics and the base plate.
- Fabrication can be simple if water jacket is manufactured by drilling holes through the base plate and plugging the ends with grub screws.
- Final assembly is very compact and allows a PCB board to be mounted direct across the bottom of the package without cutouts for the heat exchanger.



3.5.2. Simplified thermal model of such solution



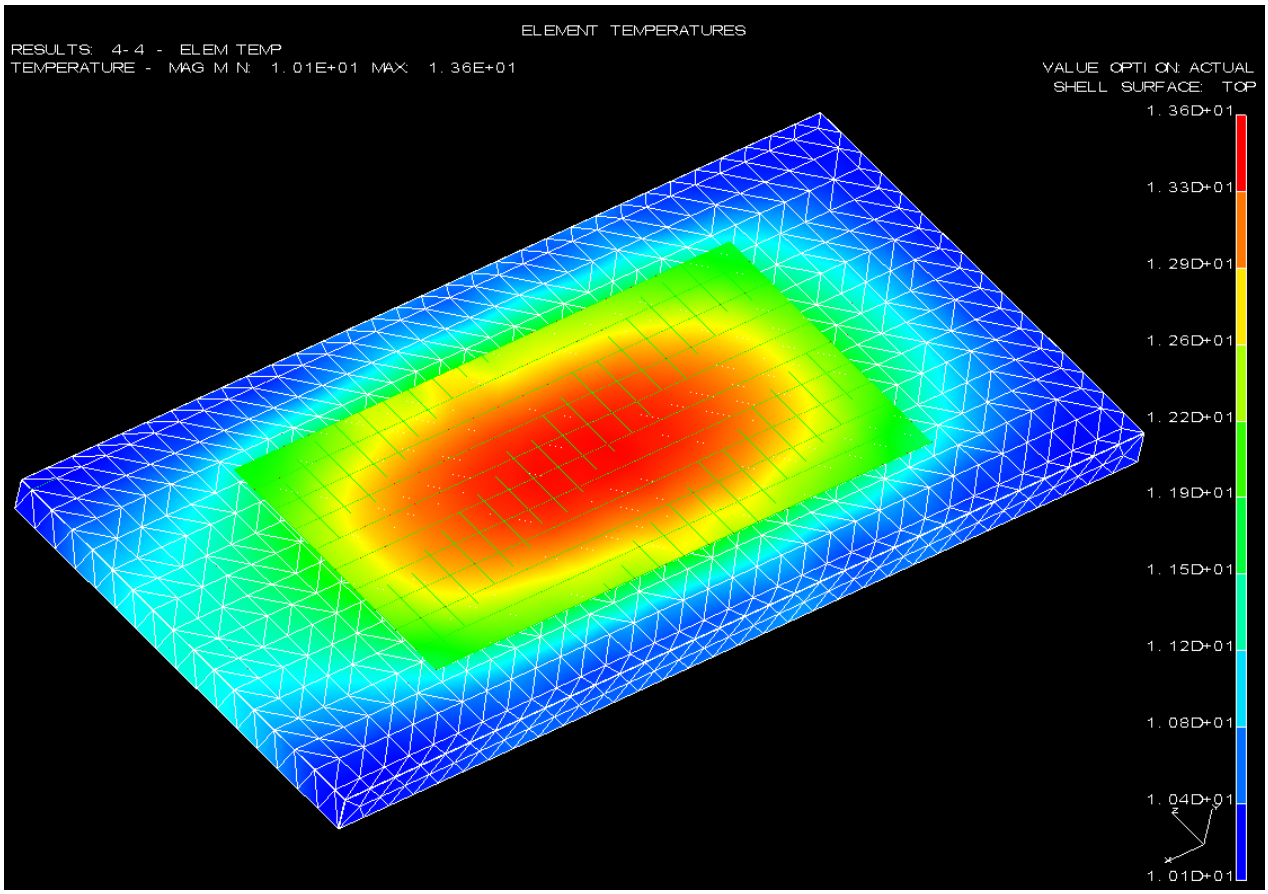
We started from the previous model, but we removed the aluminum plate separated by the Silpad foil to the Copper/tungsten package. We consider that the Peltier Package (in orange here) is still glued with 50 µm of glue.
In blue in this figure is the water cooling path: it is considered, for a thermal model simplification, that the water flow is high enough to ensure that at this interface, the temperature is the water temperature (10°C). This water path has a width of 2 mm.

The goal of this thermal model is to check if this cooling circuit is sufficient to ensure a nominal cooling of the package.

3.5.3. Thermal model of alternative design 1

We keep here the copper/tungsten plate proposed by e2v.

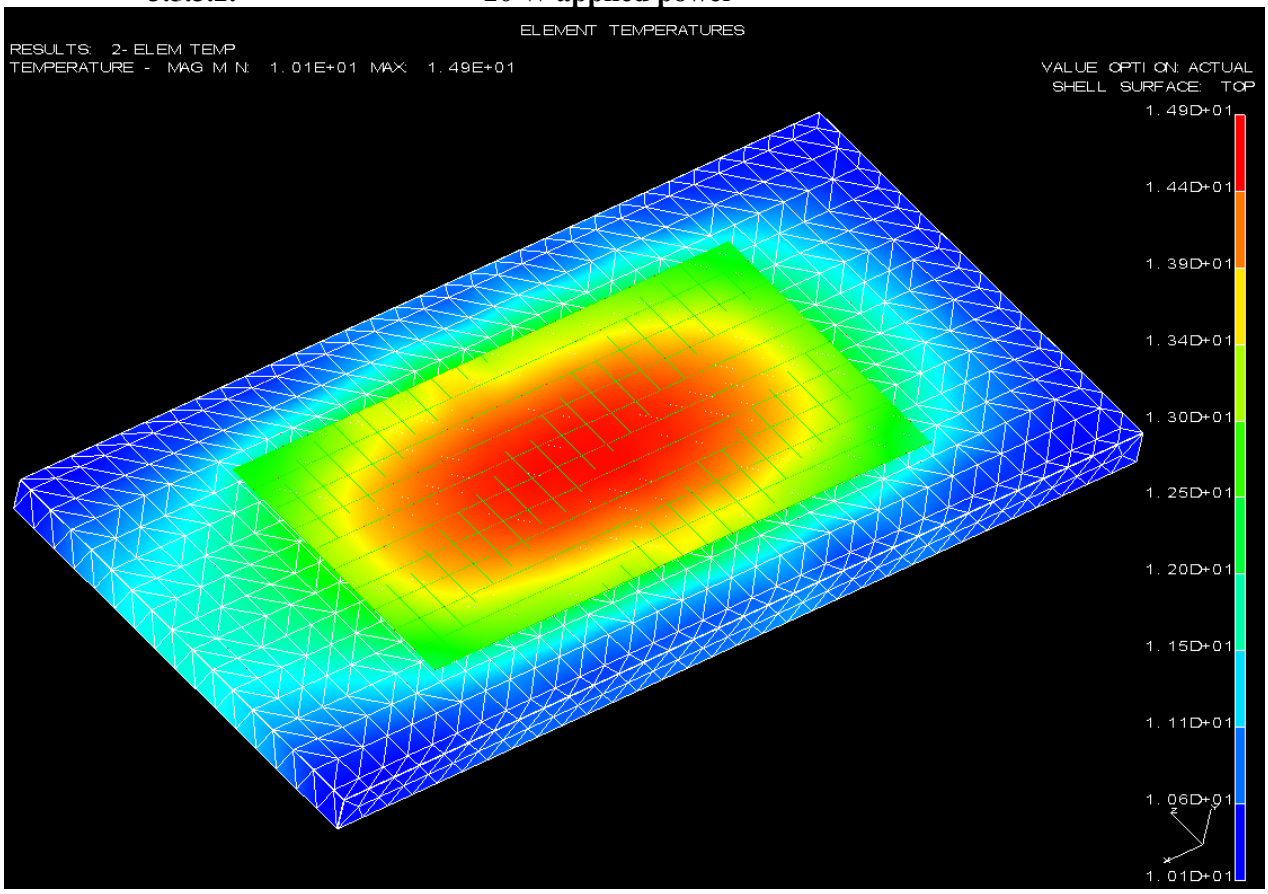
3.5.3.1. 15W applied power



Min	Max	Average
11.51	13.67	12.87

$$R_{th} = \frac{T_{av}(°C) - 10}{15} = 0.191\,°\text{C/W}$$

3.5.3.2. 20 W applied power



Min	Max	Average
12.02	14.89	13.83

$$R_{th} = \frac{T_{av}(°C) - 10}{20} = 0.191\,°C/W$$

The thermal resistance is higher in this case: 0.191 °C/W instead of 0.125 °C/W.
This is due to:

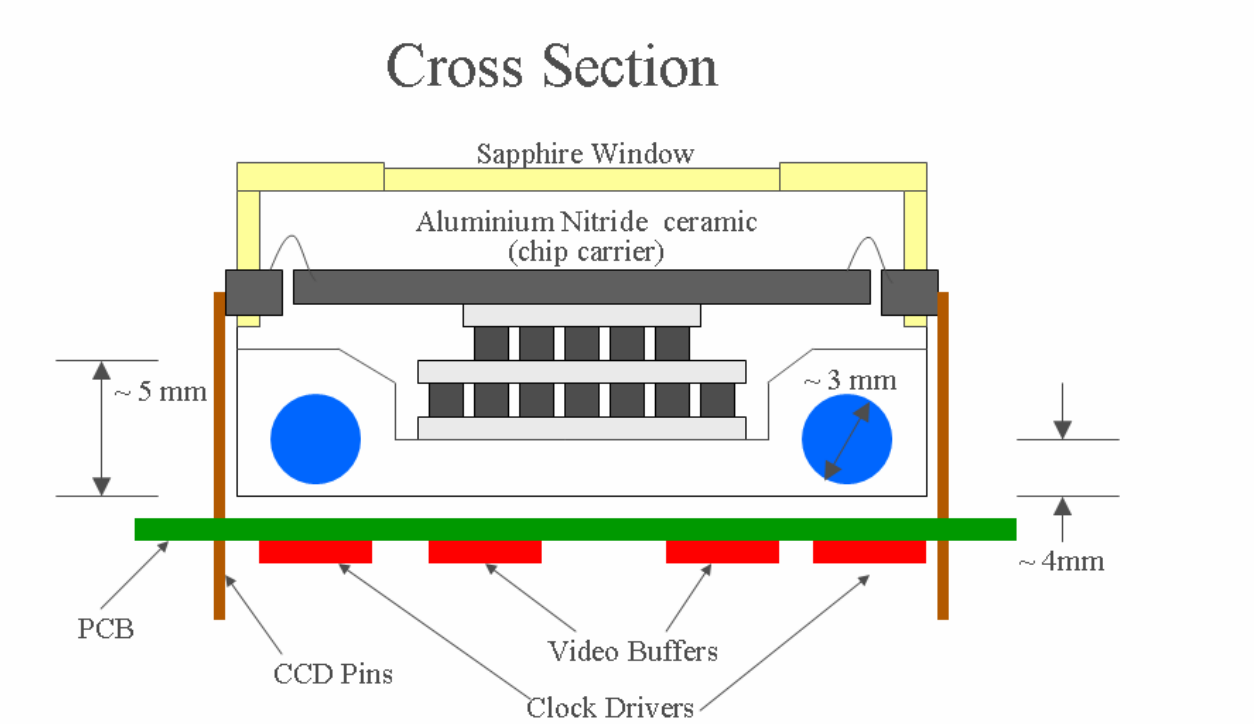
- The relatively "poor" thermal conductivity of the Copper/tungsten base and a thickness which is not high enough.
- The area of the water cooling exchanger which is not high enough and which is not spread on the entire area of the back plate of the package.

3.5.4. Conclusion for the alternative design 1

This design can not be used like this because thermal performances are limited. Some improvements to this design were considered in an "alternative design 2", see next section.

3.6. Alternative design 2

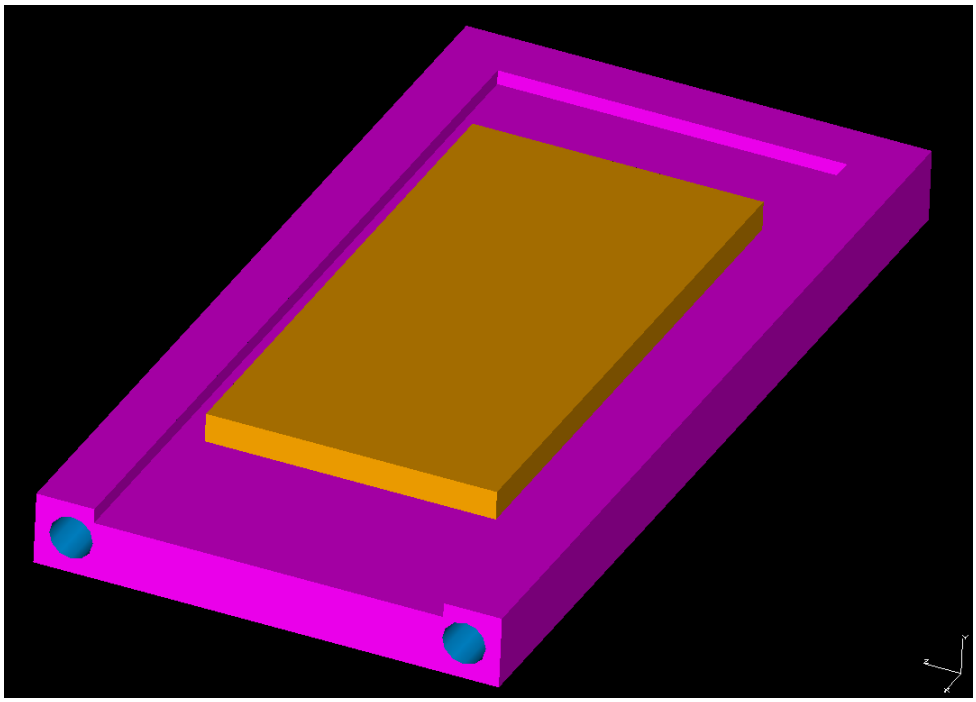
3.6.1. Purpose and geometry



To avoid the disadvantages of the previous concept (alternative design 1), the following changes were made:
- increase of the thickness under the Peltier from 2.5 to 4 mm.
- increase of the diameter of the water tubes from 2 to 3 mm.
The base of the package is still made of Copper/tungsten having a thermal conductivity of 190 W/m-K.

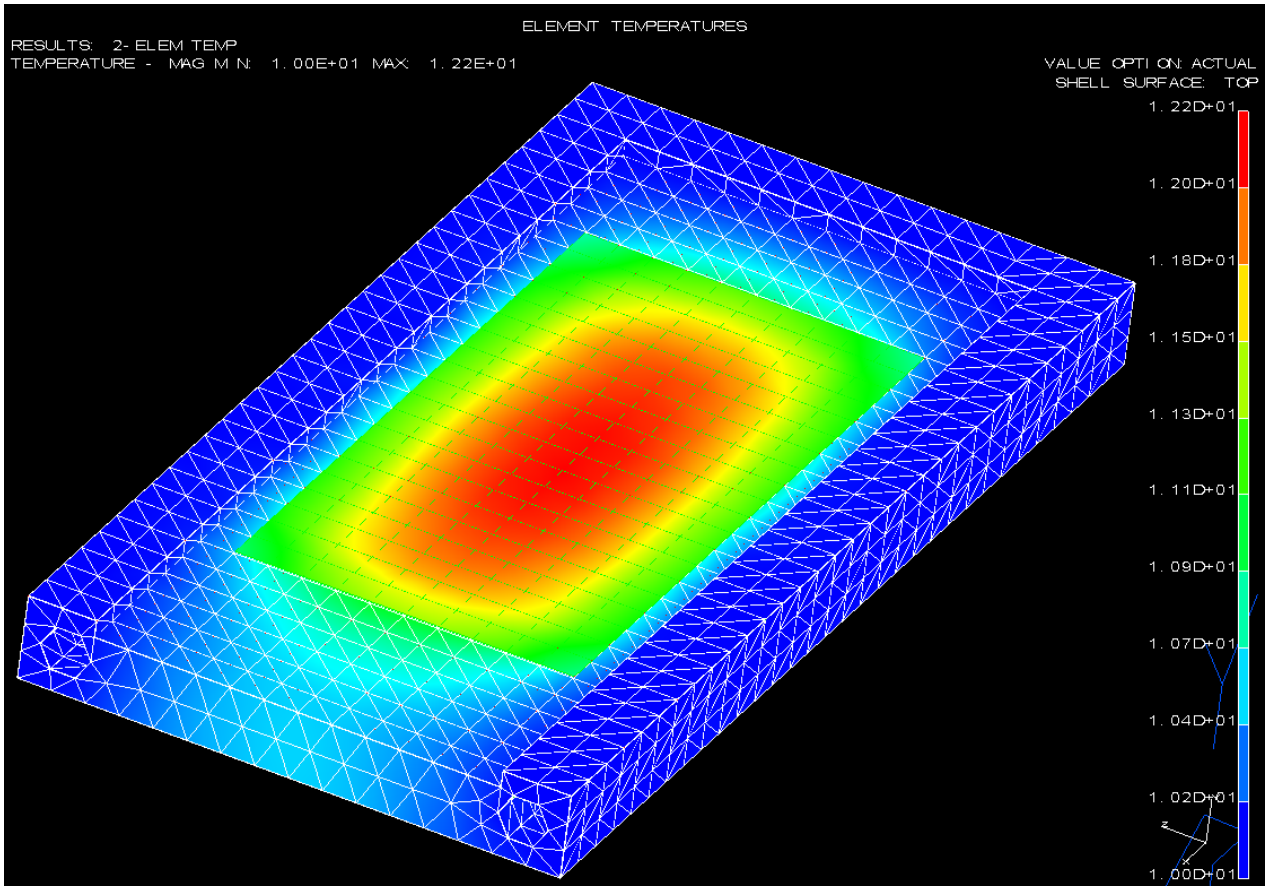
3.6.2. Thermal model of alternative design 2

To increase the precision of the model, a real 3D model of the plate was done with the water tube included inside as in the conceptual cross section of the previous paragraph. The water tube is 3 mm in diameter and is located at the borders of the Copper/Tungsten plate. There is 1 mm of Cu/tungsten material between the water tube and the border of the package. This base was meshed with 3D elements.
To facilitate thermal modelling, it was considered that the inner surface of the water tube is at 10°C, which means that the water flow is high enough to ensure that this hypothesis is true. Further work is needed to model the thermal exchange by forced convection between the tube and the water. The TMG software allows this kind of modelling.
The following figure shows the 3D model that was used for the thermal modelling of this concept. The water tube, in blue, can be seen on this figure:



3.6.2.1. 15W applied power

With 15W applied power, we obtained the following results:



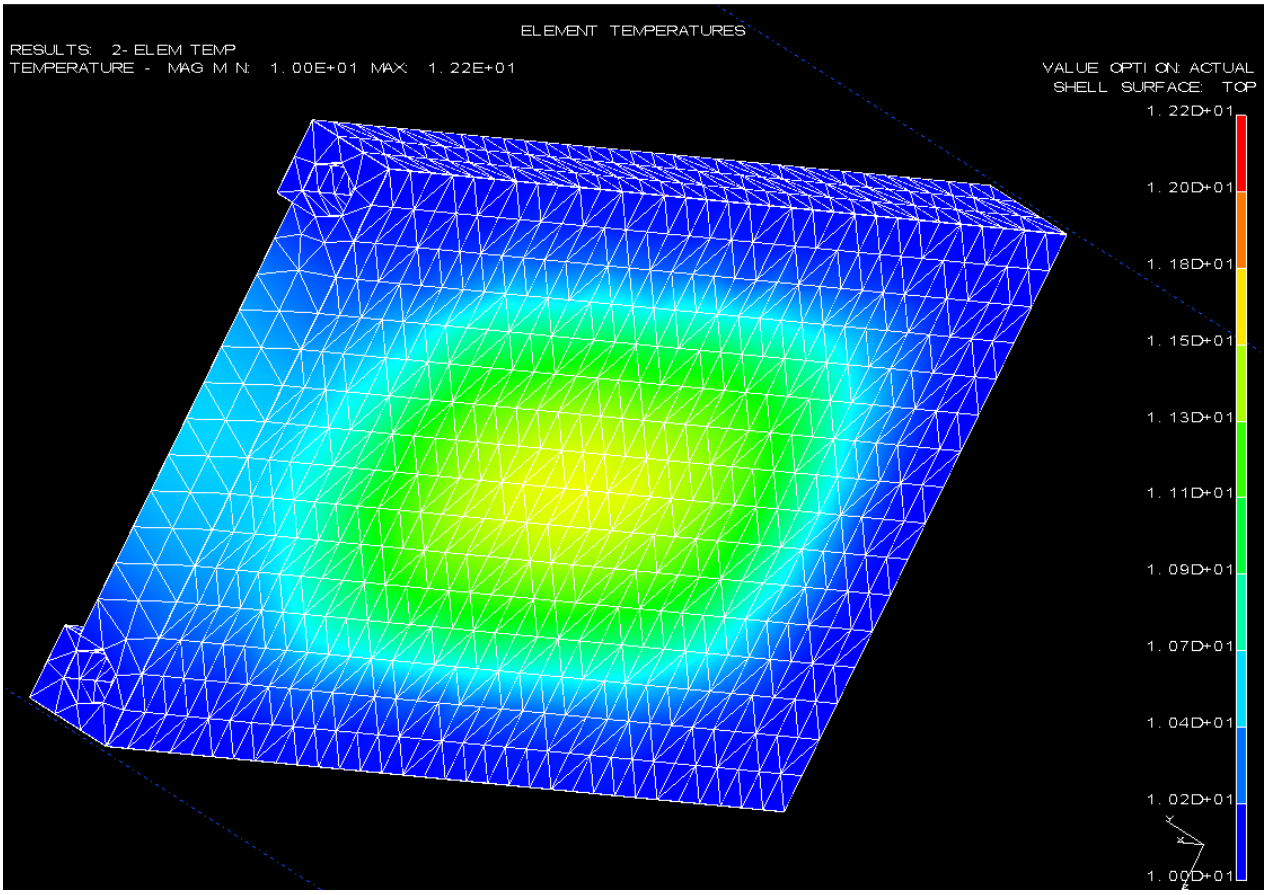
At the interface glue/peltier, one has the following temperatures:

Min	Max	Average
10.75	12.21	11.66

From this, an "equivalent" thermal resistance can also be calculated:

$$R_{th} = \frac{T_{av}(°C) - 10}{15} = 0.111\,°C/W$$

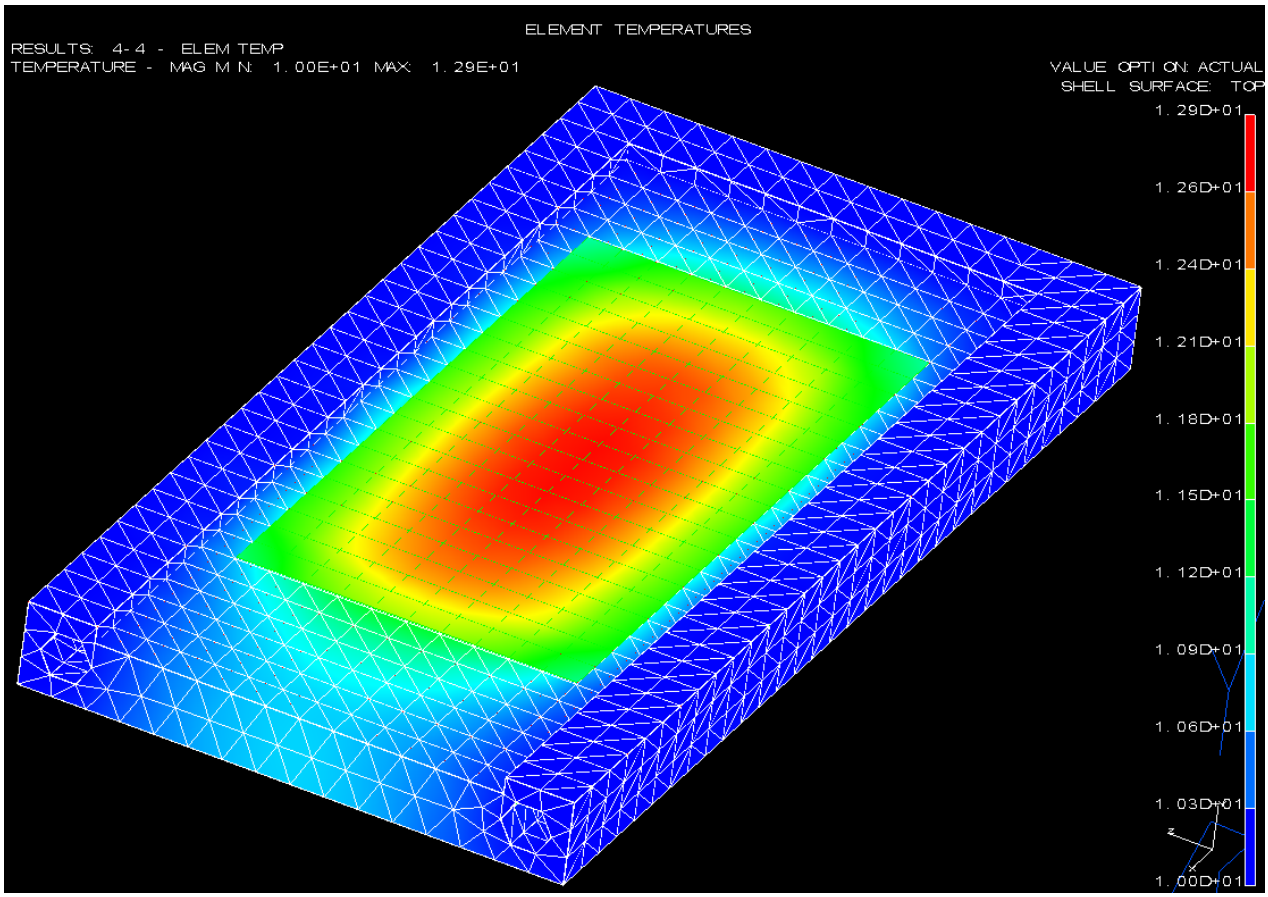
Note that in that case, the temperature of the back side of the package is not uniform, due to the non uniformity of the water cooling, as it can be seen on this figure:



A temperature gradient of about 1.5K can be seen at the back side of the package.

1.1.1.1 20W applied power

With 20W applied power, we obtained the following results:



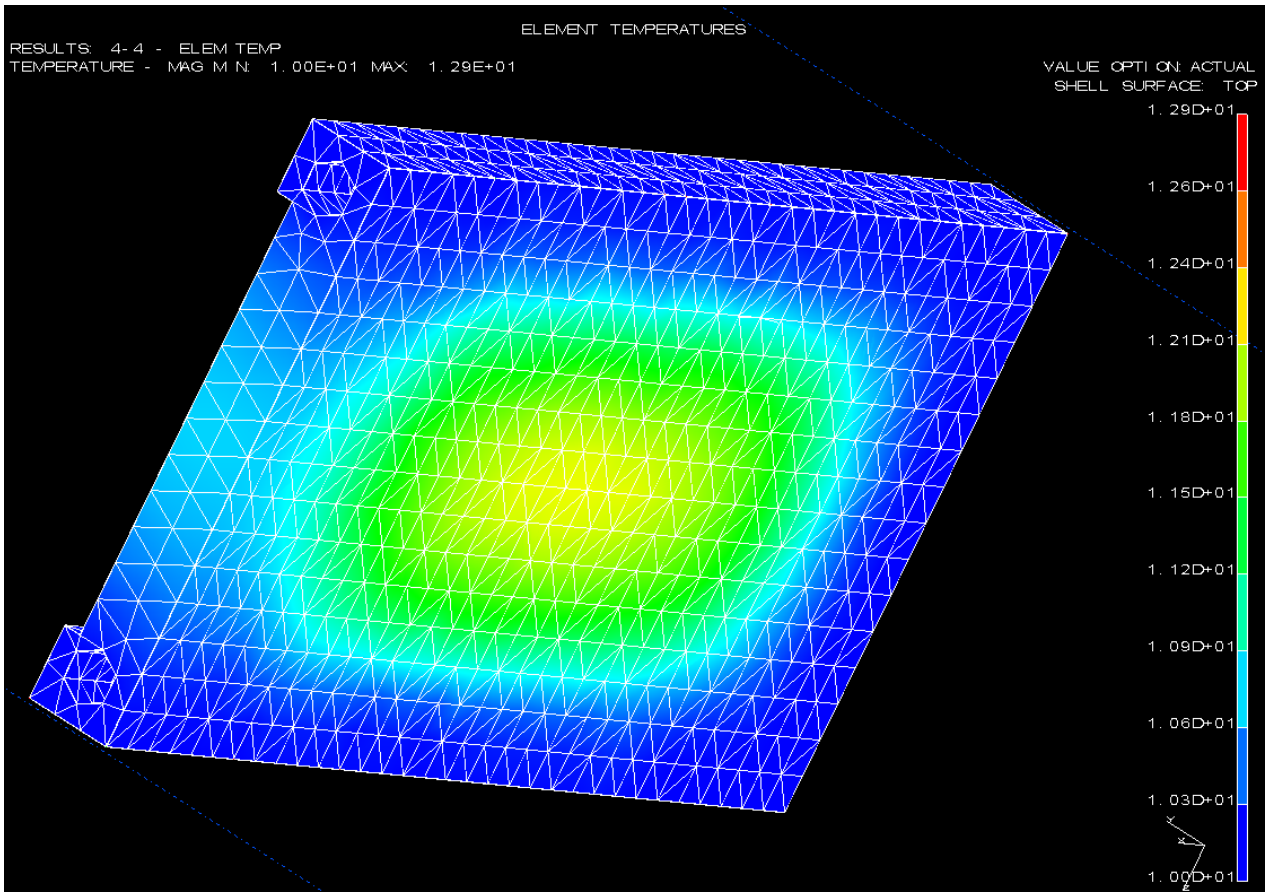
At the interface glue/Peltier, one has the following temperatures:

Min	Max	Average
11.00	12.95	12.22

From this, an "equivalent" thermal resistance can also be calculated:

$R_{th} = \frac{T_{av}(°C) - 10}{20} = 0.111 °C/W$ (Same result than with 15W).

The back side of the package shows a temperature gradient of about 2K:



3.6.3. Conclusion for the alternative design 2

This design is very attractive, because:

- It shows good thermal performances with a thermal resistance of 0.111 °C/W. Note that the real thermal resistance should be close to this value, because the number of interfaces is reduced in this concept.
- design compact, simple, reliable
- Minimize wire lengths, which is a major advantage compared to the original concept.
- Use the same copper/tungsten material that was considered in the original concept.

Nonetheless, if this concept is chosen, some further work is needed:

- A thermal model of the package performances as a function of the water flow is needed, in order to verify that these performances are not obtained with a turbulent flow that could generate vibrations.
- From a more general point of view, because the water flow is just under the detector, the vibration impact should be analyzed. Note that this remark is also true with the original concept.
- For this concept, the maximum Delta T that is foreseen for the package is between 2.2 and 3 K, depending on the power applied (15 to 20 W).

4. CONCLUSION FOR THE WP4 ACTIVITY

The activity of the WP4 encountered no technical issues, the final concept for the cryogenic system will be chosen at the Detector Design Review of September 2005. The chosen solution will be compact, reliable and extremely simple to operate.

Detector testing work package (WP5) activity report

1- SCOPE OF THIS ACTIVITY

The goal of this work package is to evaluate the performances of the fabricated detector in the framework of AO wavefront sensors.
Although this work package has not formally started, documents have been produced to organize this important activity. Tests will be shared between the manufacturer (for the most important tests) and the Opticon consortium, for more exotic tests.
The test plan is for e2v to do parametric and functional tests and measure standard parameters such as noise, gain, cosmetics, dark current, smearing, and CTE and for IAC (Canary Islands) and ESO to do full acceptance tests plus measure the more exotic parameters such as crosstalk, PRNU, fringing, and PSF.

2- APPLICABLE DOCUMENTS

AD5 Test Equipment Requirements, VLT-SPE-E2V-14690-0002, issue 2, 27th May 2005.

AD6 CCD Test Plan, VLT-PLA-E2V-14690-0008, issue 1, 25th May 2005

3- THE OPTICON (ESO) CONTRIBUTION TO THE CONTRACT WITH E2V

To reduce testing costs, ESO will loan E2V, detector test equipment. The system will be capable of reading out the sensor in all required operating modes in order to perform detector read out tests as outlined in the detector test plan. No commissioning of this equipment is foreseen by E2V. At project close-off, the test equipment will be returned to ESO.
The test equipment will consist of a complete electronic CCD controller, capable of driving the sensor and acquiring image frames and a suitable detector head, with agreed interface to E2V's optics. The electronics will include a control and acquisition PC capable of storing data frames (images) in FITS format.
The delivery of this test equipment will be by best effort. There is a small possibility that the delivery of this equipment will be delay for up to 6 months. This delay may impact E2V's schedule such that subsequent milestones are delay by an equivalent period of time.
It is agreed that E2V shall NOT give any information about the controller to a third party company.
The test equipment, for which ESO is responsible, is then subcontracted inside the Opticon consortium, with the following responsibilities:
- the detector controller is under the responsibility of LAM, laboratory from INSU/CNRS (content of the WP3).
- the cryogenic system is under the responsibility of the LAOG, laboratory from INSU/CNRS (content of the WP4).

4- TESTS UNDER THE RESPONSABILITY OF THE E2V MANUFACTURER

Using the camera head (controller and cryogenic system), the e2v manufacturer is responsible for the demonstration of the minimum requirements that are listed in the contract (see AD1). The mains tests that will be performed by e2v are listed here:

- DC probe test
- Basic functional test before CCD packaging under tungsten-halogen illumination.
- Technology characterisation: Peltier package performances, electro-optical tests (functional image test, gain characteristics, multiplication register test, dark signal, speed and frame rate, full well capacity, cosmetics, traps, noise, linearity, smear, charge transfer efficiency…), selection of delivered detectors.

5- TESTS UNDER THE RESPONSIBILITY OF THE OPTICON CONSORTIUM

The Opticon consortium will test the detector in more exotic conditions. By example, e2v plan to test the detector at 1.2 kframe/sec, the Opticon consortium will test it at 1.5 kframe/sec.

Conclusions and perspectives

1. SCIENTIFIC CONCLUSIONS

The JRA2 encountered no major issues since the beginning of the Opticon contract. The whole activity was delayed by about 6 months due mainly to the late signature of the contract and the late availability of the funding.
The partnership between the participants of the consortium is excellent, all the institutes are working very well together with well defined tasks and interfaces.
A subcontract for the design, fabrication and delivering of the detector was signed between ESO and e2v. The device delivery is scheduled by the second quarter of 2007. This development is jointly funded by Opticon and ESO.
Although the developed detector is challenging, we adopted a low risk profile in order to end this activity with a usable detector fully dedicated to the next generation of AO systems.
The partnership with the e2v manufacturer is also very fruitful, e2v accepted guaranteed and goal performances. Regular project meetings with e2v are planned and general meetings for the JRA2 are also organized.
To save funding, it was also decided to use the same camera head (controller and cryogenic system) than the one that will be developed by the Opticon consortium. As a consequence, this head will be loaned to e2v during the test period at e2v. These tests will be further completed at IAC suing the same camera head (test equipment).

2. FUNDING

2.1. Generalities

The entire funding of the JRA2 is needed during the FP6 contract of Opticon. Indeed, the detector development is now sub-contracted to the e2v manufacturer since March 2005. This contract was issued under the ESO responsibility and was approved by late 2004 by the ESO finance committee. The deal with this contact is complex because ESO (through the Opticon consortium) has the responsibility to deliver the camera head, called "test equipment" in the contract. Delaying the delivering of the camera to e2v would delay by the same amount the contract with e2v until a certain limit. Not delivering this camera, due to a lack of funding by example, could even stop the contract with e2v with no refunds of what was expensed.

2.2. Expenses by Work Package

2.2.1. WP1 Management and WP3 Cryogenic system

No hardware expenses made on the WP3 until now. Work consisted in discussions and simulations only. An additional contract between LAOG (INSU/CNRS), responsible for WP3, and e2v is foreseen for the delivering of a Peltier package having improved performances. This contract will be funded by the funding available at LAOG for the WP3.

Expenses for the WP1 (responsible LAOG INSU/CNRS):

Amount asked for the period	46500 €
Funding delivered to INSU/CNRS for the WP4	46500 €
Charges (INSU/CNRS and LAM)	- 5 487 €
Delivered to the WP1 and WP3	41 013 €
Expenses in 2004	2 020.06 €
Expenses in 2005 (until end June 2005)	4623.76 €
Balance for WP1 and WP3 (June 2005)	32 425.59 €

2.2.2. WP2 Detector

Purchase Order P/O 004379 dated March 31, 2005 to E2V Technologies Ltd for CCD detectors at the price of EUR 1 119 500.
The total payment made until now against this order amounts to EUR 223 900.

2.2.3. WP4 Detector controller

Amount asked for the period	37 000 €
Funding delivered to INSU/CNRS for the WP4	31875 €
Charges (INSU/CNRS and LAM)	- 4875 €
Delivered to the WP4	27000 €
Expenses in 2004	9243.41 €
Expenses in 2005 (until end June 2005)	24996.44 €
Balance (June 2005)	-7239.85 €

As it can be noted, the balance for this WP is negative, the delivering of the 2005 funding is now urgent, mainly for this WP.

2.2.4. WP5 Detector testing

Not formally started during the reporting period (as foreseen).

3. PERSPECTIVES: ADDITIONNAL ACTIVITIES FOR THE FUTURE?

Because the JRA2 has some common objectives with the JRA3, we could think to:

- join some objectives of the JRA3 WP2 (EMCCD developments) with the JRA2 developments. The detectors produced within the JRA2 are potentially of great interest for the JRA3. Additional JRA2 devices could be produced by e2v on request for evaluation within the JRA3. The cost of this operation has to be estimated.
- participate to the JRA3 WP3 (P-N sensor development): ESO is strongly interested by the P-N sensor technology although this company did not answered to the JRA2 call for tender. ESO could provide additional funding to P-N sensor in order to test the

low-noise high speed device that is produced. This technology can compete with the EMCCD technology of e2v and is of great interest for AO wavefront sensors.

- APD array developments (JRA3 WP4): again this development could interest AO systems and we are interested to follow this technology.
- JRA3 WP5: controller development: collaboration between the JRA2 and JRA3 are interesting for a good sharing of knowledge concerning this technical aspect. For this reason, Craig Mackay from the University of Cambridge is invited to the detector Design Review at e2v in September 2005.

JRA2 papers to be published

1. P. Feautrier *et al*, "Zero noise wavefront sensor development within the Opticon European network", proceedings of the Scientific Detector Worshop 2005, Taormina June 2005, Springer editions, editors: P.Amico and J. Beletic.
2. M. Downing *et al*, "A Dedicated L3CCD for Adaptive Optics Applications", proceedings of the Scientific Detector Worshop 2005, Taormina June 2005, Springer editions, editors: P.Amico and J. Beletic.
3. J-L. Gach *et al*, "A dedicated controller for Adaptive Optics L3CCD developments", proceedings of the Scientific Detector Worshop 2005, Taormina June 2005, Springer editions, editors: P.Amico and J. Beletic.